MESFET Distributed Amplifier Design Guidelines

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Abstract—In this paper, the analysis of GaAs MESFET distributed amplifiers and a systematic approach to their design are presented. The analysis focuses on fundamental design considerations and also establishes the maximum gain–bandwidth product of the amplifier. The design approach presented enables one to examine the tradeoffs between the variables, such as the device, the number of devices, and the impedances and cutoff frequency of the lines, and arrive at a design which gives the desired frequency response. Excellent agreement is shown when the theoretically predicted response of a typical amplifier is compared with computer-aided analysis results, and good agreement is shown with previously published experimental results.

I. INTRODUCTION

THE PRINCIPLE of distributed or traveling-wave amplification using discrete transistors is a technique whereby the gain–bandwidth product of an amplifier may be increased. In this approach, the input and output capacitances of the transistors are combined with lumped inductors to form artificial transmission lines. These lines are coupled by the transconductances of the devices. The amplifier can be designed to give a flat, low-pass response up to very high frequencies.

Distributed amplifiers using discrete FET's have been demonstrated at microwave frequencies [1]–[5]. The traveling-wave transistor, an interesting variation of the discrete FET distributed amplifier, has also been proposed [6]. However, we will show in this paper that the discrete FET distributed amplifier, unlike the traveling-wave transistor, can be designed to give flat response nearly up to the cutoff frequency of the lines.

The topology of the distributed amplifier is particularly suited to MMIC's because its passive circuit predominantly consists of inductors which can be realized in the form of short lengths of microstrip lines. Recently, broad-band MMIC distributed amplifiers using GaAs MESFET's have been presented [1]–[3]. The design of the distributed amplifier involves a careful choice of the variables, such as the device, the number of devices, and the impedances and cutoff frequency of the lines, to obtain the desired frequency response. Even though several distributed amplifiers using MESFET's have been built, a systematic design approach which enables one to examine the tradeoffs between the design variables has not been presented.

The distributed amplifier has been extensively analyzed since it was first proposed in 1937 by Percival [7]. We present here only a limited sample of literature [8]–[12]. The unified analysis of Chen [12] treats a general case distributed amplifier composed of image matched, nonuniform input and output transmission lines and is the most complete analysis currently available.

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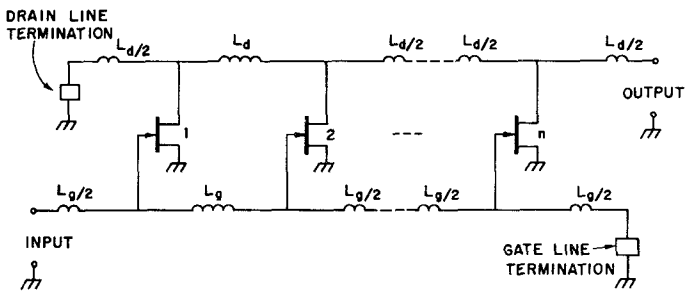

Fig. 1. Schematic of FET distributed amplifier.

In this paper, we analyze the MESFET distributed amplifier by focussing on fundamental design considerations and present a graphical design approach which enables one to examine the tradeoffs between the design variables and arrive at a design under the constraint of maximum gain–bandwidth product. The design approach will be illustrated by an example and the analytically predicted response will be compared with the results obtained by computer-aided circuit analysis. We will also compare the predicted response of a typical amplifier with previously published experimental results.

II. AMPLIFIER ANALYSIS

A schematic representation of the FET distributed amplifier is shown in Fig. 1. The gate and drain impedances of the FET's are absorbed into lossy artificial transmission lines formed by using lumped inductors as shown. The resultant transmission lines are referred to as the gate and drain lines. The lines are coupled by the transconductances of the FET's.

An RF signal applied at the input end of the gate line travels down the line to the terminated end, where it is absorbed. As the signal travels down the gate line, each transistor is excited by the traveling voltage wave and transfers the signal to the drain line through its transconductance. If the phase velocities on the gate and drain lines are identical, then the signals on the drain line add in the forward direction as they arrive at the output. The waves traveling in the reverse direction are not in phase, and any uncancelled signal is absorbed by the drain-line termination.

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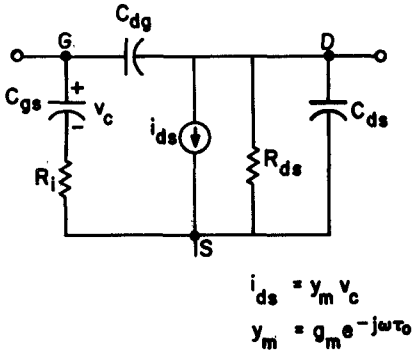

Fig. 2. Simplified equivalent circuit of a MESFET.

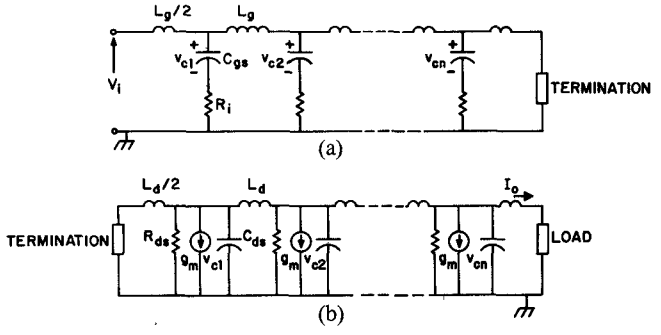

Fig. 3. (a) Gate transmission line. (b) Drain transmission line.

A simplified equivalent circuit of a MESFET arrived at from typical S-parameter measurements at microwave frequencies [3] is shown in Fig. 2. R_i is the effective input resistance between the gate and source terminals and C_{gs} is the gate-to-channel capacitance. R_{ds} and C_{ds} are the drain-to-source resistance and capacitance, respectively. C_{dg} is the drain-to-gate capacitance and g_m the transconductance. In our analysis, the device will be considered unilateral and C_{dg} will be neglected.

The equivalent gate and drain transmission lines are shown in Fig. 3(a) and (b). They are essentially loaded constant-k lines, wherein the parasitic resistances of the FET's are considered the dominant loss factors. The lines are assumed to be terminated in their image impedances at both ends. The current delivered to the load is given by

$$I_0 = \frac{1}{2} g_m e^{-\theta_d/2} \left[\sum_{k=1}^{n} V_{ck} e^{-(n-k)\theta_d} \right] \tag{1}$$

where V_{ck} is the voltage across C_{gs} of the kth transistor and $\theta_d = A_d + j\Phi_d$ is the propagation function on the drain line. A_d and Φ_d are the attenuation and phase shift per section on the drain line. n is the number of transistors in the amplifier.

V_{ck} can be expressed in terms of the voltage at the gate terminal of the kth FET as [13]

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j\tan^{-1}(\omega/\omega_g)}}{\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]} \tag{2}$$

where V_i is the voltage at the input terminal of the amplifier and $\theta_g = A_g + j\Phi_g$ is the propagation function on the gate line. A_g and Φ_g are the attenuation and phase shift per section on the gate line, $\omega_g = 1/R_i C_{gs}$ is the gate-circuit radian cutoff frequency, and $\omega_c = 2\pi f_c$ is the radian cutoff frequency of the lines. For constant-k type transmission lines, the phase velocity is a well-known function of the cutoff frequency f_c of the line. By requiring gate and drain lines to have the same cutoff frequency, the phase velocities are constrained to be equal. Therefore, we have $\Phi_g \simeq \Phi_d = \Phi$ [13]. From (1) and (2), I_0 can be expressed as

$$I_0 = \cdot \frac{g_m V_i \sinh\left[\frac{n}{2}(A_d - A_g)\right] e^{-n(A_d+A_g)/2} e^{-jn\Phi - j\tan^{-1}(\omega/\omega_g)}}{2\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]\sinh\left[\frac{1}{2}(A_d - A_g)\right]}. \tag{3}$$

The power delivered to the load and input power to the amplifier are given, respectively, by

$$P_0 = \frac{1}{2}|I_0|^2 \mathrm{Re}[Z_{ID}] \simeq \frac{1}{2}|I_0|^2 \sqrt{L_d/C_d\left[1-(\omega/\omega_c)^2\right]}$$

and

$$P_i = \frac{|V_i|^2}{2|Z_{IG}|^2} \mathrm{Re}[Z_{IG}] \simeq \frac{1}{2}|V_i|^2 \Big/ \sqrt{L_g/C_g\left[1-(\omega/\omega_c)^2\right]}$$

where Z_{ID} and Z_{IG} are the image impedances of the drain and gate lines [13].

Therefore, the power gain of the amplifier is

$$G = \frac{g_m^2 R_{01} R_{02} \sinh^2\left[\frac{n}{2}(A_d - A_g)\right] e^{-n(A_d+A_g)}}{4\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]\left[1-(\omega/\omega_c)^2\right]\sinh^2\left[\frac{1}{2}(A_d - A_g)\right]} \tag{4}$$

where $R_{01}(=\sqrt{L_g/C_g})$ and $R_{02}(=\sqrt{L_d/C_d})$ are the characteristic resistances of the gate and drain lines, respectively.

Consider an ideal impedance transformer at the output port which transforms R_{02} to the gate-line characteristic resistance R_{01} of the succeeding amplifier in a tandem connection of identical amplifiers. Then, from (4), the magnitude of the voltage gain of a single amplifier stage can be shown to be

$$A = \frac{g_m (R_{01}R_{02})^{1/2} \sinh\left[\frac{n}{2}(A_d - A_g)\right] e^{-n(A_d+A_g)/2}}{2\left[1+\left(\frac{\omega}{\omega_g}\right)^2\right]^{1/2}\left[1-\left(\frac{\omega}{\omega_c}\right)^2\right]^{1/2}\sinh\left[\frac{1}{2}(A_d - A_g)\right]}. \tag{5}$$

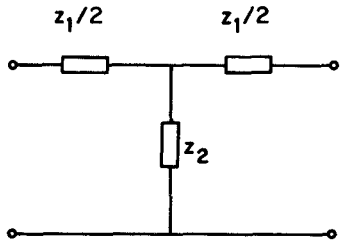

Fig. 4. A section of constant-k line.

From (5), one can show that the number of devices which maximizes gain at a given frequency is [14]

$$N_{\text{opt}} = \frac{\ln(A_d/A_g)}{A_d - A_g}. \tag{6}$$

A similar relation was found by Podgorski and Wei [6] for the optimum gate width of a traveling-wave transistor. Therefore, it is clear that in the presence of attenuation, the gain of a distributed amplifier cannot be increased indefinitely by adding devices. This property of the distributed amplifier can be easily explained. As the signal travels down the gate line, each transistor receives less energy than the previous one due to attenuation on the gate line. Similarly, the signal excited in the drain line by a transistor is attenuated by the subsequent line sections between it and the output port. Therefore, additional transistors not only decrease the excitation of the last device but also increase the overall attenuation on the drain line. The gain of the amplifier increases with additional devices until the optimum number of devices at the given frequency is reached. Any device added beyond the optimum number is not driven sufficiently to excite a signal in the drain line which will overcome the attenuation in the extra section of the drain line. Consequently, the gain of the amplifier begins to decrease with further addition of devices.

A. Attenuation on Gate and Drain Lines

The attenuation on gate and drain lines is the critical factor controlling the frequency response of the amplifier, as will be shown. The expressions for gate- and drain-line attenuations can be derived from the propagation function for the constant-k line, which is given by the relation [15]

$$\cosh(A + j\Phi) = 1 + \frac{Z_1}{2Z_2}. \tag{7}$$

Z_1 and Z_2 are the impedances in the series and shunt arms of a section of constant-k line as shown in Fig. 4, and A and Φ are the attenuation and phase shift per section of the line. When attenuation per section is small (≤ 0.4 Np), one can derive from (7) the following expressions for attenuation on gate and drain lines [13]:

$$A_g = \frac{(\omega_c/\omega_g)X_k^2}{\sqrt{1-\left[1-\left(\frac{\omega_c}{\omega_g}\right)^2\right]X_k^2}} \tag{8}$$

$$A_d = \frac{\omega_d/\omega_c}{\sqrt{1-X_k^2}} \tag{9}$$

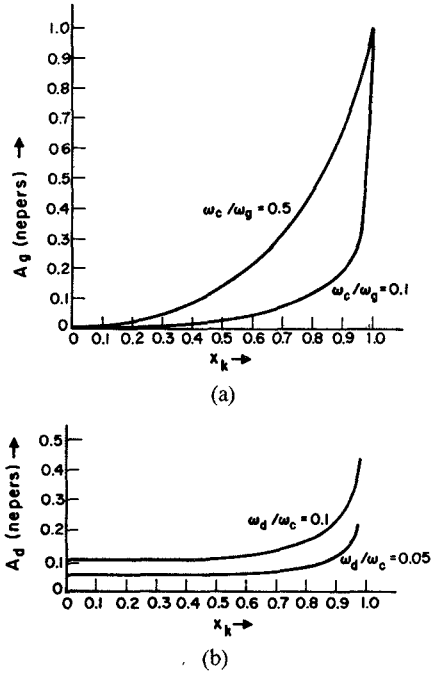

Fig. 5. (a) Attenuation on gate line versus normalized frequency. (b) Attenuation on drain line versus normalized frequency.

where $X_k = \omega/\omega_c$ is the normalized frequency

$$\omega_g = 1/R_i C_{gs}, \quad \omega_d = 1/R_{ds} C_{ds}$$

and

$$\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} = \frac{2}{\sqrt{L_d C_{ds}}}.$$

The attenuation on gate and drain lines versus frequency with ω_c/ω_g and ω_d/ω_c as parameters are shown in Fig. 5(a) and (b), respectively. It is evident from the figures that the gate-line attenuation is more sensitive to frequency than drain-line attenuation. Further, unlike attenuation in the gate line, the drain-line attenuation does not vanish in the low-frequency limit. Therefore, the frequency response of the amplifier can be expected to be predominantly controlled by the attenuation on the gate line and the dc gain by the attenuation on the drain line, as will be shown in the following section.

It is clear from (8) and (9) that attenuation on the gate and drain lines can be decreased by making ω_c/ω_g and ω_d/ω_c small. Therefore, for a given ω_c, one has to choose a device having high ω_g and low ω_d.

B. Frequency Response

Extending the analysis of Horton *et al.* [9], (8) and (9) can be rewritten as

$$A_g = \frac{2aX_k^2}{n\sqrt{1+\left[\frac{4a^2}{n^2}-1\right]X_k^2}} \tag{10}$$

$$A_d = \frac{2b}{n\sqrt{1-X_k^2}} \tag{11}$$

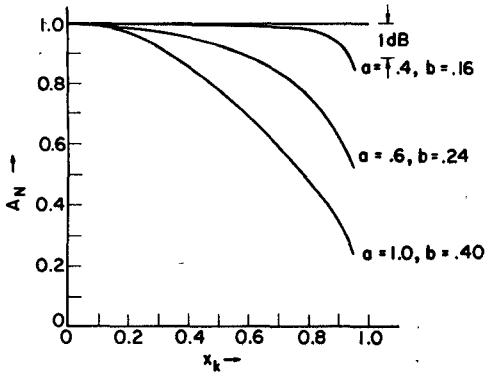

Fig. 6. Normalized frequency response of MESFET distributed amplifiers.

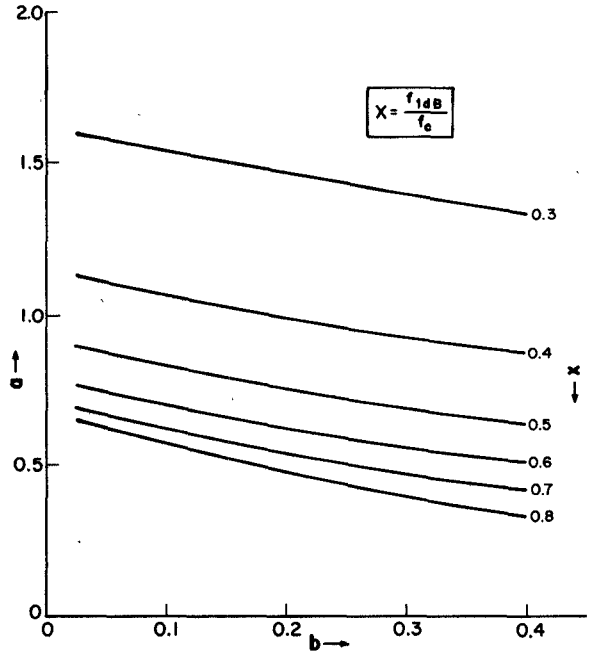

Fig. 7. Fractional bandwidth curves.

where

$$a=\frac{n\omega_c}{2\omega_g} \tag{12}$$

and

$$b=\frac{n\omega_d}{2\omega_c}. \tag{13}$$

Using (10) and (11), one can derive from (5) the following expression for the normalized gain:

$$A_N=\frac{A}{A_0}$$
$$=\frac{\sinh\left(\frac{b}{n}\right)e^{b}\sinh\left[b/\left(1-X_k^2\right)^{1/2}-ax_k^2/\left[1+\left(\frac{4a^2}{n^2}-1\right)X_k^2\right]^{1/2}\right]e^{-[b/(1-X_k^2)^{1/2}+ax_k^2/[1+(4a^2/n^2-1)X_k^2]^{1/2}]}}{\sinh(b)\left[1+\frac{4a^2}{n^2}X_k^2\right]^{1/2}\left[1-X_k^2\right]^{1/2}\sinh\frac{1}{n}\left[b/\left(1-X_k^2\right)^{1/2}-aX_k^2/\left[1+\left(\frac{4a^2}{n^2}-1\right)X_k^2\right]^{1/2}\right]} \tag{14}$$

where A_0, the dc gain (the gain of the amplifier in the low-frequency limit), is given by

$$A_0=\frac{g_m(R_{01}R_{02})^{1/2}\sinh(b)e^{-b}}{2\sinh(b/n)}. \tag{15}$$

It is evident from (14) that the normalized frequency response (normalized gain versus normalized frequency) of the amplifier is a function of the parameters a, b, and n. The a and b parameters are related to gate- and drain-line attenuations, respectively. The dc gain of the amplifier is controlled by the attenuation on the drain line as seen in (15).

From (14), one can determine the normalized frequency response of the amplifier for various values of a and b, as shown in Fig. 6. The value of n used is 4. For given values of a and b, the normalized response does not change appreciably with n, for n greater than 4. Therefore, the normalized frequency response of the amplifier is completely characterized by the parameters a and b. We will show later how the a and b values are related to a particular circuit.

By a proper choice of a and b parameters, the amplifier can be designed to give a nearly flat response up to a frequency close to the cutoff frequency of the lines. This is the distinct advantage of the distributed amplifier using discrete transistors as compared to a traveling-wave transistor proposed by Podgorski and Wei [6], whose gain monotonically decreases due to transmission-line attenuation. In the case of a distributed amplifier using discrete transistors, the rise in voltage at the gate terminals compensates to some extent the effect of gate-line attenuation as the cutoff frequency is approached (see (2)). This can be seen if one views the lumped constant gate line as cascaded π-sections. The transistor gate–source terminals are connected across the π-section terminals. It is well known that the image impedance of a π-section, and hence the gate-source voltage, rises as the cutoff frequency is approached. How this effect can be used to obtain nearly flat low-pass response out to frequencies approaching the cutoff of the lines will be demonstrated.

In order to enable cascading of distributed amplifier stages, the individual amplifiers must be designed to give a nearly flat gain response up to the desired maximum frequency. This calls for an appropriate choice of a and b parameter values. An ideal frequency response is the one which is flat up to the cutoff frequency of the lines. However, depending on the values of a and b, the frequency response starts deviating from the ideal response at a frequency below the cutoff frequency of the lines. In order to select the required frequency response and corresponding a and b values, it is necessary to characterize these

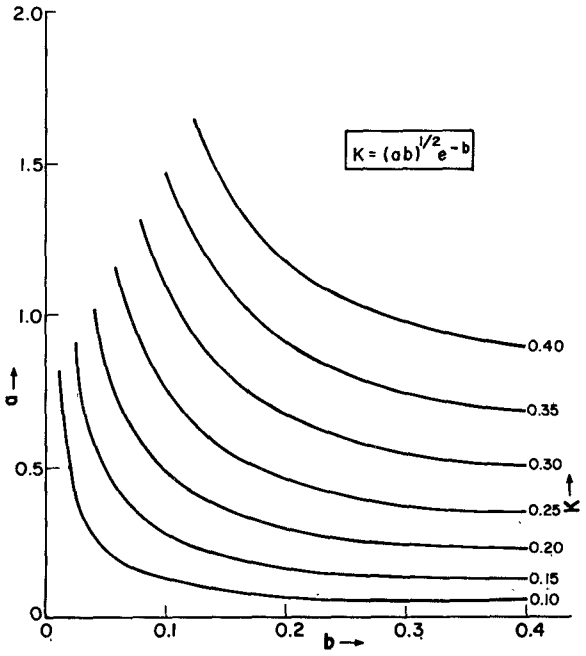

Fig. 8. K = const. curves.

responses by their degrees of flatness. We define the degree of flatness as the fractional bandwidth $X = f_{1\,\mathrm{dB}}/f_c$, where $f_{1\,\mathrm{dB}}$ is the frequency at which the gain of the amplifier falls below the dc gain by 1 dB, as shown in Fig. 6.

The values of parameters a and b which give the same fractional bandwidth can be determined from (14) by iteration, and are plotted on the $a-b$ plane as shown in Fig. 7. These curves give the designer the values of a and b to choose from which yield the same fractional bandwidth. It is clear from Fig. 7 that the flatness of response is quite sensitive to the parameter a, which controls the attenuation on the gate line.

C. Gain–Bandwidth Product

One can derive the following relation starting from (15) when $b \leqslant 0.4$, [13]:

$$\frac{A_0 f_c}{4 f_{\max}} = (ab)^{1/2} e^{-b} \tag{16}$$

where $f_{\max}$ is the frequency at which the maximum available gain (MAG) of the FET becomes unity [16]. It is also referred to as the maximum frequency of oscillation of the FET. $f_{\max}$ is given by

$$f_{\max} \simeq \frac{g_m}{4\pi C_{gs}} \sqrt{\frac{R_{ds}}{R_i}}\,. \tag{17}$$

Equation (16) can be expressed as

$$A_0 f_{1\,\mathrm{dB}} = 4KX f_{\max} \tag{18}$$

where $K = (ab)^{1/2}e^{-b}$ and $f_{1\,\mathrm{dB}} = X f_c$. Fig. 8 shows K = const. curves on the $a-b$ plane. Equation (18) gives the gain–bandwidth product of a MESFET distributed amplifier. It is dependent on the values of a and b, as well as the $f_{\max}$ of the FET. For a given MESFET, $f_{\max}$ is fixed. Therefore, (18) gives the gain–bandwidth product of the amplifier for the chosen values of a and b.

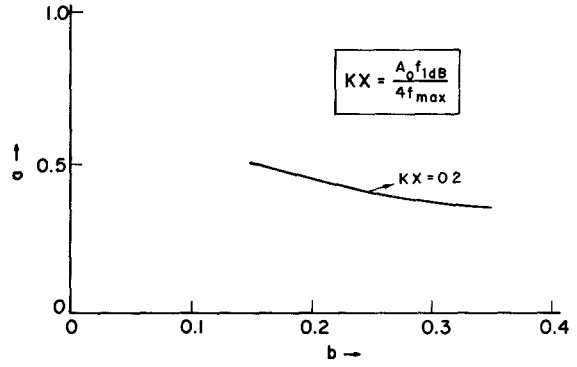

Fig. 9. Normalized maximum gain–bandwidth product curve.

The factor KX in (18) can be viewed as the gain–bandwidth product of the amplifier normalized to $4f_{\max}$. The value of KX can be found from Figs. 7 and 8. The maximum value can be shown to be about 0.2. Fig. 9 shows the normalized maximum gain–bandwidth product curve on the $a-b$ plane. By choosing the parameter values a and b to lie on this curve, one can design a distributed amplifier having maximum gain–bandwidth product.

It follows that the maximum gain–bandwidth product is given by

$$A_0 f_{1\,\mathrm{dB}} \simeq 0.8 f_{\max}. \tag{19}$$

It can be seen that the maximum gain–bandwidth product of the distributed amplifier is constrained by the $f_{\max}$ of the device. From (19), one can show that the frequency at which the gain of the distributed amplifier becomes unity cannot exceed $0.7 f_{\max}$. We have also confirmed this by the computer-aided analysis of several distributed amplifiers.

III. Amplifier Design

Up to this point, we have shown how the frequency response of the amplifier depends on a range of values of the parameters a and b, and we will now show how the choices of cutoff frequency and impedances of the lines, and particular active device and their number constrain the values of a and b and hence the frequency response. The systematic design approach presented below will enable one to examine the possible tradeoffs between the design variables and arrive at a suitable design.

The following relations can be derived from (12) and (13):

$$ab = \frac{n^2 \omega_d}{4\omega_g} \tag{20}$$

$$a/b = \frac{\omega_c^2}{\omega_g \omega_d}. \tag{21}$$

Equation (20) defines the value of the product ab in terms of the number of devices and the device characteristic frequencies (ω_g and ω_d). This equation defines a family of hyperbolas on the $a-b$ plane as shown in Fig. 10. Equation (21) defines a family of lines on the $a-b$ plane as shown in Fig. 10. Each line corresponds to a cutoff frequency (f_c) and characteristic resistances (R_{01} and R_{02})

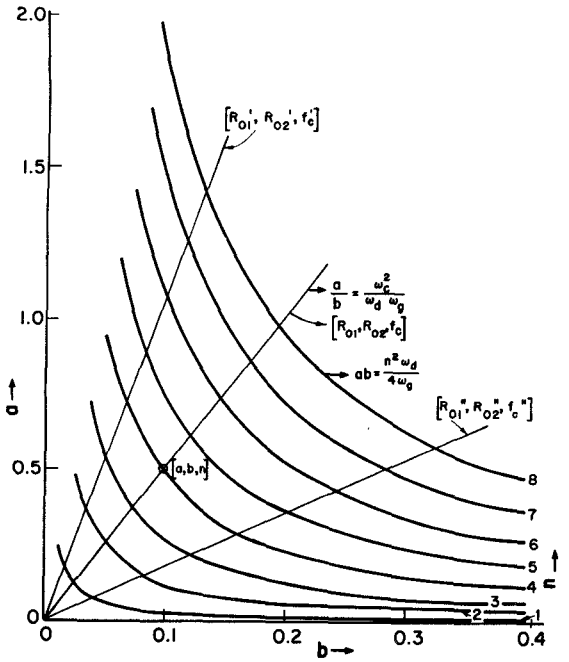

Fig. 10. ab = const. curves and a/b = const. lines.

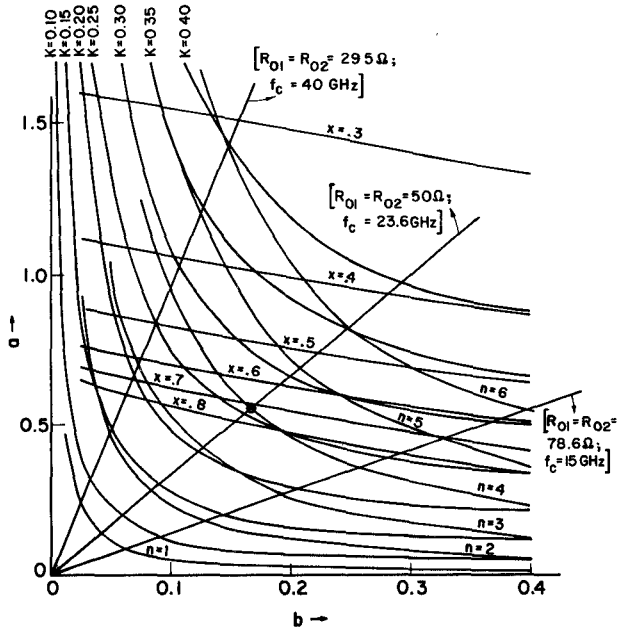

Fig. 11. Design curves for the distributed amplifier using typical 300-μm MESFET's.

of the lines because they are related as follows:

$$R_{01} = \frac{1}{\pi f_c C_{gs}}, \quad R_{02} = \frac{1}{\pi f_c C_{ds}}$$

$$f_c = \frac{1}{\pi\sqrt{L_g C_{gs}}} = \frac{1}{\pi\sqrt{L_d C_{ds}}}.$$

The point of intersection of a hyperbola defined by (20) and a line defined by (21) determines an operating point on the $a-b$ plane. The value of X (fractional bandwidth) and K corresponding to this operating point can be obtained from Figs. 7 and 8, respectively, since the coordinates (a, b) of the point are known. Then the dc gain (A_0) and bandwidth $(f_{1\,\mathrm{dB}})$ can be obtained from the following relations:

$$f_{1\,\mathrm{dB}} = Xf_c \tag{22}$$

$$A_0 = \frac{4KXf_{\max}}{f_{1\,\mathrm{dB}}}. \tag{23}$$

The frequency response of the amplifier can be obtained from (14). The amplifier is now completely defined in terms of the device, the number of devices, the cutoff frequency and the impedances of the lines, and the frequency response. Superposition of Figs. 7, 8, and 10 will enable one to examine the tradeoffs between the design variables. We will now illustrate the design approach presented above by an example.

A. Design Example

Let us consider the design of a distributed amplifier using typical 300-μm MESFET's which have the following characteristic frequencies:

$$f_g = \omega_g/2\pi = 84.2 \text{ GHz}$$

$$f_d = \omega_d/2\pi = 4.8 \text{ GHz}$$

$$f_{\max} = 77.2 \text{ GHz}.$$

Let $R_{01} = R_{02}$. Therefore, we have $C_{gs} = C_{ds} + C_p$, since the cutoff frequencies of the lines are also constrained to be equal. C_p is an external capacitance added to the device output capacitance C_{ds}. For the MESFET considered here, $C_{gs} = 0.27$ pF, $C_{ds} = 0.11$ pF, and $R_{ds} = 300\ \Omega$. Therefore, we obtain the following equations:

$$f_d' = 1/2\pi R_{ds}(C_{ds} + C_p) = 1.96 \text{ GHz} \tag{24}$$

$$ab = \frac{n^2\omega_d'}{4\omega g} = (5.82\times10^{-3})n^2 \tag{25}$$

$$a/b = \frac{\omega_c^2}{\omega_d'\omega_g} = (6.06\times10^{-21})f_c^2. \tag{26}$$

The set of design curves consisting of curves defined by (25), the lines defined by (26), fractional bandwidth curves (Fig. 7), and K = const. curves (Fig. 8) are plotted on the $a-b$ plane as shown in Fig. 11. For an amplifier having $R_{01} = R_{02} = 50\ \Omega$, $f_c = 23.6$ GHz, and $n = 4$, we obtain the following values for a, b, X, and K from Fig. 11:

$$a = 0.56$$
$$b = 0.17$$
$$X = 0.7$$
$$K = 0.25.$$

Therefore, the bandwidth of the amplifier is

$$f_{1\,\mathrm{dB}} = Xf_c = 16.52 \text{ GHz}$$

and the dc gain is

$$A_0 = \frac{4KXf_{\max}}{f_{1\,\mathrm{dB}}} = 3.27\ (10.29 \text{ dB}).$$

The frequency response of this amplifier predicted by (14) and the response obtained by using the standard microwave circuit analysis program are shown in Fig. 12. They are in good agreement. The image terminations are realized

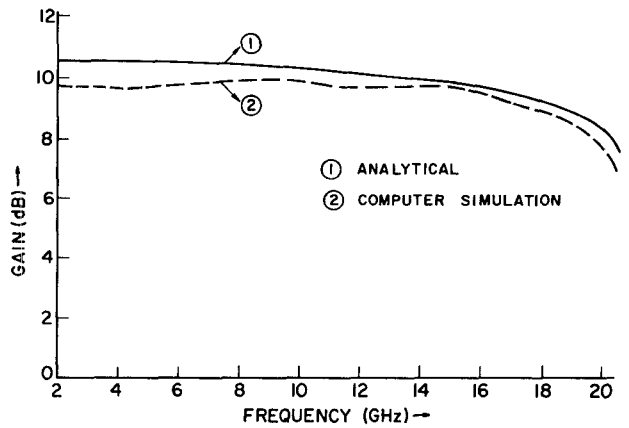

Fig. 12. Frequency response of the four-section distributed amplifier using typical 300-μm MESFET's.

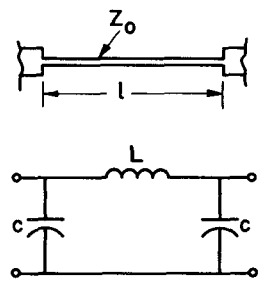

Fig. 13. A short length of microstripline and its equivalent circuit.

by using the standard m-derived filter half sections at both ends of the lines [13].

A careful study of Fig. 11 reveals that for a given cutoff frequency (and hence the impedance of the lines), the gain of the amplifier can be increased by adding devices at the expense of bandwidth. On the other hand, if the number of devices is decreased, one can obtain a larger bandwidth by sacrificing gain. If the number of devices is fixed, a decrease in cutoff frequency (and hence an increase in the impedance of the lines) results in an increase in gain and reduction in bandwidth.

B. Some Practical Design Considerations

Design of a distributed amplifier as discussed in this paper involves the design of the lumped inductors. As already mentioned, the lumped inductors can be realized by short lengths of high-impedance microstripline. A short length of microstripline and its equivalent circuit are shown in Fig. 13.

For a short length $l(<\lambda_g/7)$ of loss-free line, the inductance is given by

$$L \simeq \frac{Z_0 l}{\lambda_g f} \tag{27}$$

where Z_0 is the characteristic impedance of the microstripline, f is the frequency, and λ_g is the wavelength in the microstripline. The end capacitances are given by

$$C \simeq \frac{l}{2fZ_0\lambda_g}. \tag{28}$$

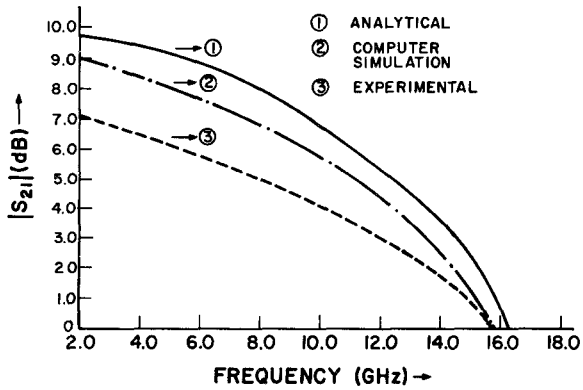

Fig. 14. Frequency response of the six-section distributed amplifier.

The end capacitances can be absorbed into gate and drain lines by taking them into account in the design of the transmission lines. For a given Z_0 and highest frequency of operation, the restriction on l limits the maximum realizable value of inductance. Even though it is advantageous to increase Z_0 in order to achieve high inductance and low end capacitance values, a practical limit is reached when the width of the microstrip becomes too small, resulting in excessive attenuation in the microstrip. Also, the geometrical considerations in the layout of the amplifier place a lower limit on the length of the inductors [13].

Another important consideration in the design of microstrip inductors is the electromigration of the metal at high current densities. In order to prevent electromigration, the current density in the microstrip should be kept below a critical value, which is of the order of $10^5 A/cm^2$ for gold. This requirement places an additional restriction on the design of microstrip inductors if they must carry dc current to bias the FET's.

The measured frequency response of a distributed amplifier [3] is shown in Fig. 14. The figure also shows the responses predicted analytically and by computer-aided analysis. The analytically predicted response was obtained by applying corrections for input and output reflection coefficients and attenuation due to series resistance of the inductors. The analytically predicted frequency response is in good agreement with the response obtained by computer-aided analysis. The discrepancy between the computer-simulated and measured responses was attributed to additional losses in source grounding bars in the amplifier, and slight differences between the test FET's and the FET's in the amplifier [17].

IV. Conclusions

The analysis of MESFET distributed amplifiers and a systematic approach to their design has been presented. The analysis has revealed that the transmission-line attenuation caused by the device parasitic resistances is the critical factor in the design of the amplifier. The analysis has also shown that the gain–bandwidth product of the distributed amplifier can only approach the f_{max} of the individual device. The graphical design approach presented enables one to examine the tradeoffs between the variables,

such as the device, the number of devices, and cutoff frequency and impedances of the lines, and arrive at a design which gives the desired frequency response.

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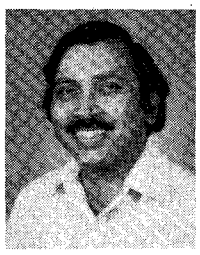

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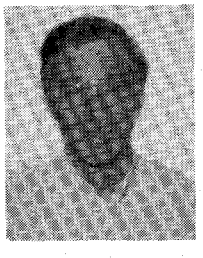

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